Md Yekra Rahman

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Education

Bangladesh University of Engineering and Technology (BUET) — Dhaka, Bangladesh
Bachelor of Science in Electrical and Electronic Engineering; ***GPA: 3.65/ 4.00*** — *April 2018 – May 2023*

Relevant Coursework: Analog Integrated Circuits, Power Electronics, Microprocessors and Embedded Systems, Control Systems, Digital Signal Processing, Digital Logic Design, VLSI Circuits and Design, Power System I, Processing and Fabrication Technology, Electrical Properties of Materials, Solid State Devices, Compound Semiconductor Devices, Optoelectronics, Nano-electronics and Nanotechnology, Electrical Circuits, Electronic Circuits, Computer Programming

Skills/Strengths

Analog and Digital Circuit Design: Cadence, Quartus, Proteus, PSpice
Materials and devices : Quantum Espresso, Materials Studio, Lumerical FDTD, SCAPS 1D
Data Analysis and automation: MATLAB, Python, Microsoft Excel, Google Spreadsheet
Miscellaneous: C, Keil, arm, Simulink, GUI, Arduino, PSAF, Latex, AppSheet, Microsoft Office

Professional Experience

Graduate Teaching Assistant — August 2024 – Present
University of Texas at Dallas — *Richardson, TX, USA*

Course Assisted: Probability Theory and Statistics

Lecturer — August 2023 – August 2024
Eastern University — *Dhaka, Bangladesh*

Courses Instructed: Power System Analysis, Signals and Linear Systems, Electric and Magnetic Field, Digital Logic Design Lab, Electronics II Lab, Electrical Service Design

Research Interests

Signal Processing, Machine Learning, Smart Grids, Renewable Energy Systems, Energy Optimization, Power System Stability

Research Experience & Publications

Undergraduate Thesis — May 2022 – May 2023

Publication: Md Yekra Rahman, Sharif Mohammad Mominuzzaman. *"Exploring Lead-Free Mixed Halide Double Perovskites Solar Cell"*, 13th International Conference on Electrical and Computer Engineering (ICECE 2024), Dhaka, Bangladesh, December 2024. (Accepted for Publication)

Projects

Phase Locked Loop: Design and Implementation | *GitHub* | *Website*

- Designed a phase-locked loop circuit using Cadence tools, constructing each component with the analog library from scratch.
- Created essential blocks to complete the circuit, including Phase Frequency Detector, Charge Pump, Current-Starved Voltage-Controlled Oscillator, and Frequency Divider.

DC-DC Buck Converter Design | *Website*

- Analyzed MOSFET parameters $R_{ds(on)}$, Q_{oss}, and Q_g to design power stage.
- Developed a 12 V/1 V and 1 A with optimized output ripple voltage and inductor current DC-DC converter using half-bridge topology with gate drivers, level shifters, dead-time generators, and bootstrapping circuits in Cadence Virtuoso utilizing tsmc 180 nm technology.

Single-Phase Sinewave Inverter | *GitHub*

- Designed a Single-Phase Sinewave Inverter using H-bridge switching topology and SPWM signals.
- Simulated the circuit in Proteus to validate the model, created a realistic model using SimScape Module of Simulink and built a hardware prototype at the PCB level.

Automated Traffic Control System | *Website*

- Designed an automated traffic control system for a 5-way circle, "Chankharpurl More," without using Arduino or microprocessors, employing Proteus for simulation and physically building the system using ICs and logic gates.

ECG Based Biometric Recognition | *GitHub* | *Website*

- Developed a biometric recognition system using ECG signals to authenticate individuals.
- Applied Chebyshev low-pass filter, median filters, and Maximal Overlap Discrete Wavelet Transform for preprocessing and feature extraction.
- Implemented Weighted K-Nearest Neighbors algorithm with Euclidean distance for classification and validated the system using a 5-fold cross-validation technique.

RISC-V Core: Design, Verification, and Synthesis

- Designed and implemented a RISC-V architecture from scratch, including RTL work and verification using both provided and customized code.
- Utilized QuartusPrime for synthesis instead of the more commonly used Cadence software.

Investigating the Effect of HVDC Connection and Large Industrial Loads in IEEE 39-Bus Network | *Website*

- Conducted load flow analysis using the Newton-Raphson method to evaluate the impact of HVDC connections and large industrial loads.
- Designed and simulated an HVDC line between Bus-39 and Bus-9 using PSAF software, addressing voltage stability and line overloads.
- Added induction motors to emulate an industrial plant, optimizing generator outputs and integrating Static VAR Compensators (SVCs) to stabilize the system.

Awards & Achievements

- **Board-Talent Pool Scholarships:** Awarded for outstanding academic performance at the Secondary and Higher Secondary levels.
- **Dean's List Award:** Received for achieving a minimum CGPA of 3.75 in Level-2.

Leadership Skills

Badhan (Voluntary Blood Donors' Organization) *February 2022 – February 2023*
President, Kazi Nazrul Islam Hall Unit, BUET

- Organized three successful events, including warm receptions for junior batches and memorable farewells for the senior batch.
- Supervised a 17-member committee to inspire approximately 300 students to donate blood voluntarily, fostering a culture of community service.

References

Dr. Sharif Mohammad Mominuzzaman
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